General Purpose High Current NPN Transistor Array

The CA3083 is a versatile array of five high current (to 100mA) NPN transistors on a common monolithic substrate. In addition, two of these transistors (Q_1 and Q_2) are matched at low current (i.e., 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
CA3083	CA3083	-55 to 125	16 Ld PDIP	E16.3
CA3083Z (Note)	CA3083Z	-55 to 125	16 Ld PDIP* (Pb-free)	E16.3
CA3083M96	3083	-55 to 125	16 Ld SOIC Tape and Reel	M16.15
CA3083MZ (Note)	3083MZ	-55 to 125	16 Ld SOIC (Pb-Free)	M16.15
CA3083MZ96 (Note)	3083MZ	-55 to 125	16 Ld SOIC (Pb-Free) Tape and Reel	M16.15

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- High I_C . . . . 100mA (Max)
- Low $V_{CE\,sat}$ (at 50mA). . . . . 0.7V (Max)
- Matched Pair (Q_1 and Q_2)
  - V_{IO} (V_{BE} Match). ±5mV (Max)
  - I_{IO} (at 1mA) . . . . 2.5µA (Max)
- 5 Independent Transistors Plus Separate Substrate Connection
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Signal Processing and Switching Systems Operating from DC to VHF
- Lamp and Relay Driver
- Differential Amplifier
- Temperature Compensated Amplifier
- Thyristor Firing
- See Application Note AN5296 "Applications of the CA3018 Circuit Transistor Array" for Suggested Applications

Pinout

CA3083
(PDIP, SOIC)
TOP VIEW
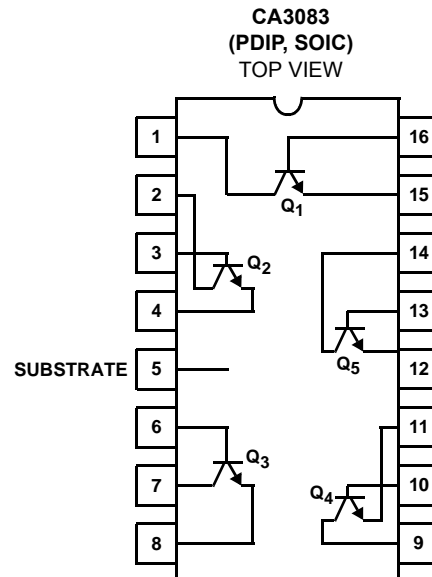
Absolute Maximum Ratings

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO} 15V

Collector-to-Base Voltage, V_{CBO} 20V

Collector-to-Substrate Voltage, V_{CIO} (Note 1). 20V

Emitter-to-Base Voltage, V_{EBO} 5V

Collector Current (I_C). 100mA

Base Current (I_B). 20mA

Operating Conditions

Temperature Range. . . . .-55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	135	N/A
SOIC Package	200	N/A

Maximum Power Dissipation (Any One Transistor) 500mW

Maximum Junction Temperature (Plastic Package) . . . . 150°C

Maximum Storage Temperature Range . . . . -65°C to 150°C

Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate Terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications   For Equipment Design, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
FOR EACH TRANSISTOR							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100µA, I_E = 0		20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100µA, I_B = 0, I_E = 0		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500µA, I_C = 0		5	6.9	-	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0		-	-	10	µA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0		-	-	1	µA
DC Forward-Current Transfer Ratio (Note 3) (Figure 1)	h_{FE}	V_{CE} = 3V	I_C = 10mA	40	76	-	
			I_C = 50mA	40	75	-	
Base-to-Emitter Voltage (Figure 2)	V_{BE}	V_{CE} = 3V, I_C = 10mA		0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage (Figures 3, 4)	$V_{CE\ SAT}$	I_C = 50mA, I_B = 5mA		-	0.40	0.70	V
Gain Bandwidth Product	f_T	V_{CE} = 3V, I_C = 10mA		-	450	-	MHz
FOR TRANSISTORS Q₁ AND Q₂ (As a Differential Amplifier)							
Absolute Input Offset Voltage (Figure 6)	$|V_{IO}|$	V_{CE} = 3V, I_C = 1mA		-	1.2	5	mV
Absolute Input Offset Current (Figure 7)	$|I_{IO}|$	V_{CE} = 3V, I_C = 1mA		-	0.7	2.5	µA

NOTE:

3. Actual forcing current is via the emitter for this test.
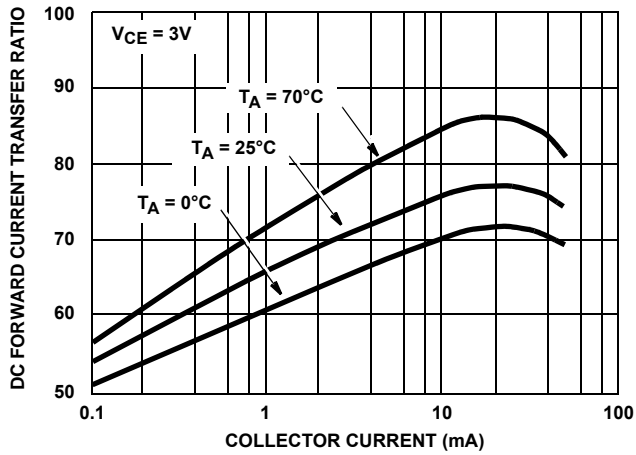
Typical Performance Curves

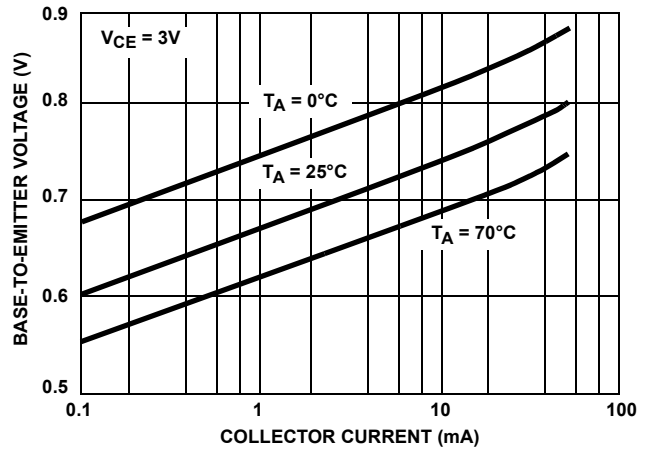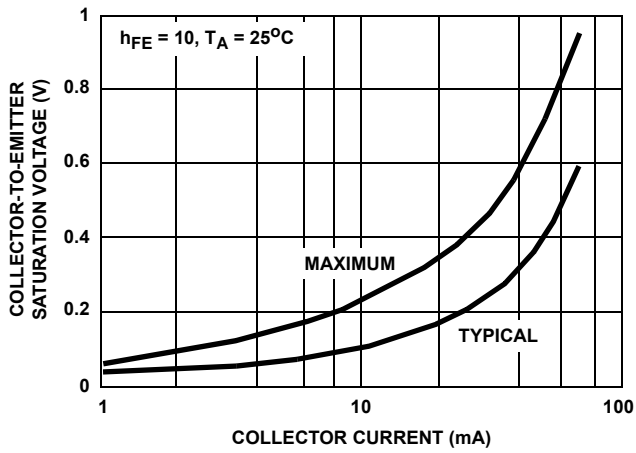FIGURE 1. h_{FE} vs I_C

FIGURE 2. V_{BE} vs I_C

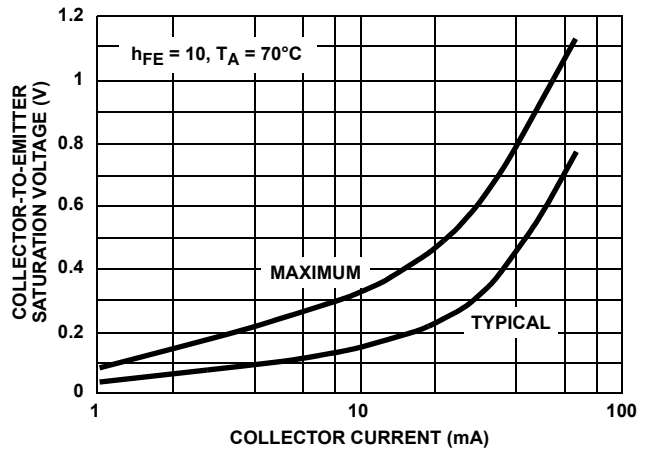FIGURE 3. $V_{CE\,SAT}$ vs I_C

FIGURE 4. $V_{CE\,SAT}$ vs I_C

FIGURE 5. $V_{BE\,SAT}$ vs I_C
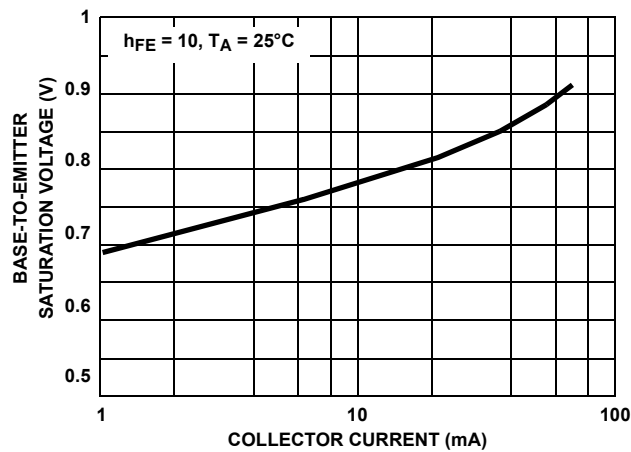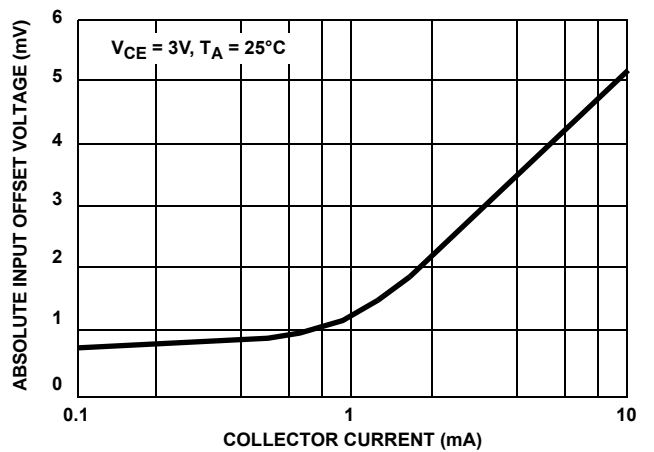

FIGURE 6. V_{IO} vs I_C (TRANSISTORS Q_1 AND Q_2 AS A DIFFERENTIAL AMPLIFIER)
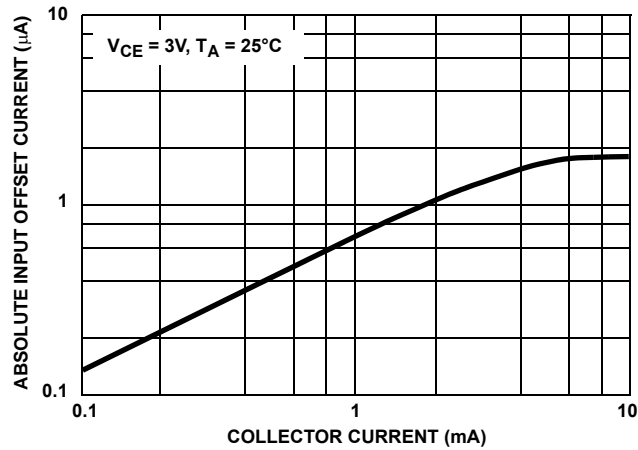
Typical Performance Curves (Continued)

FIGURE 7. I_{IO} vs I_C (TRANSISTORS Q_1 AND Q_2 AS A DIFFERENTIAL AMPLIFIER)

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

For information regarding Intersil Corporation and its products, see www.intersil.com